REMARKS

Claims 1-4 and 6-21 are presented for further examination. Claims 1, 11, and 15-20 have been amended. Claim 5 has been canceled.

In the final Office Action mailed May 12, 2009, the Examiner rejected claims 1-21 under 35 U.S.C. § 102(b) as anticipated by previously-cited Dworkin. Remarks accompanying the rejection state that the "claims do not fully differentiate the application from prior art and are rejected based on broadest reasonable interpretation."

Applicants respectfully request reconsideration and further examination of the claims.

Claim 1 has been amended to incorporate the subject matter of claim 5. In particular, claim 5 recited the apparatus including a control circuit arranged to generate individually gated clock signals for each register. Claim 11 recites the control circuit configured to selectively perform operations on data, the control circuit arranged according to the subject matter of claim 5. Similarly, claim 15 recites circuitry for controlling coupling of the data storage circuitry, the temporary data storage circuitry, and the circuitry for performing combinatorial logic operations to the read and write busses to selectively perform MD5 and SHA-1 operations on the data.

Claim 19, which is directed to a dual hash algorithm circuit, also recites the control system for selectively coupling and uncoupling the first bank and second bank of various registers to the respective read bus and the write bus to selectively perform the operations. The subject matter of claim 5 has been incorporated into this section of claim 19 so that the control circuit is more particularly defined.

All of these claims recite the generation of individual gated clock signals only for each active register, which is done by combining a master clock signal and a control signal, as described on page 7 and illustrated in Figure 2 of the present application.

As previously pointed out in prior amendments, Dworkin does not teach or suggest individually gating each of the registers to selectively perform operations and selectively coupling them to read busses and write busses in part because Dworkin does not use read busses and write busses. Rather, Dworkin sends all of the data from the registers to a summing circuit,

which is not present in the claimed embodiments of the present disclosure. Although Dworkin has a clock that controls the activity of the registers, it does so in a manner that is inapposite to the present disclosure and as recited in the claims. More particularly, the claimed embodiments of the present disclosure selectively couple the registers to the read and write busses so that only those active registers needed at that time are coupled to the read and write busses. Dworkin, in contrast, teaches coupling all of the registers to a single summing circuit as described in the paragraph referenced by the Examiner, [0011], "When a new hash value is to be computed, the values stored in these registers are initialized to specific values, and then altered **on every clock cycle** to contain chaining variables."

Dworkin at paragraph [0012] describes two modes operating in different rounds and with multiple steps with the output of the function circuit 22 connected to "a summing circuit or adder 30." Because all of the values in Dworkin's registers are altered "on every clock cycle" to contain chaining variables and sent to a single adder, there is no claimed selective coupling and uncoupling of only active registers to separate read and write busses.

In view of the foregoing, applicants respectfully submit that independent claims 1, 11, 15, and 19 are clearly novel and not anticipated by Dworkin.

Claims 2-4, 6-10, 12-14, 16-18, 20, and 21, are allowable for the features recited therein as well as for the reasons why their respective independent claims are allowable. For example, claim 20 recites the use of tristate buffers to couple each of the registers to the respective read and write busses. There is no teaching or suggestion of using individual tristate buffers with the registers in this manner in Dworkin.

In view of the foregoing, applicants respectfully submit that all of the claims in this application are clearly in condition for allowance. In the event the Examiner disagrees or finds minor informalities that can be resolved by telephone conference, the Examiner is urged to contact applicants' undersigned representative by telephone at (206) 622-4900 in order to expeditiously resolve prosecution of this application. Consequently, early and favorable action allowing these claims and passing this case to issuance is respectfully solicited.

The Director is authorized to charge any additional fees due by way of this Amendment, or credit any overpayment, to our Deposit Account No. 19-1090.

Respectfully submitted,

SEED Intellectual Property Law Group PLLC

/E. Russell Tarleton/
E. Russell Tarleton
Registration No. 31,800

ERT:alb

701 Fifth Avenue, Suite 5400
Seattle, Washington 98104
Phone: (206) 622-4900
Fax: (206) 682-6031

851663.479USPC / 1426612_1.DOC